

Fabrication of Silicon Waveguides for Near Field Coupling

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Introduction:

The field of Silicon photonics is gaining significant momentum because it allows optical devices to be cost effective using standard semiconductor fabrication techniques. It allows the integration of optical and electronic components on a single microchip. One of the problems encountered in such integration is coupling of light to the subwavelength structures. This project was inspired from the need of an efficient way to couple light to and from the subwavelength structures. Under this project two types of waveguides were studied.

1. Tapered waveguide with exponential taper^[1-2]
2. Slot waveguide with SiO₂ slot^[3-4]

The design parameters for these waveguides were finalized from FDTD simulations.

Waveguide design parameters:

1. Tapered Waveguide:

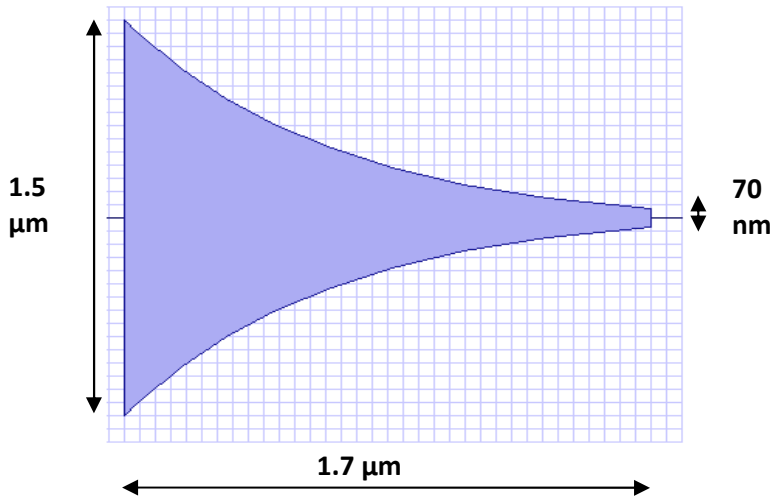


Fig. 1: Top view of tapered waveguide

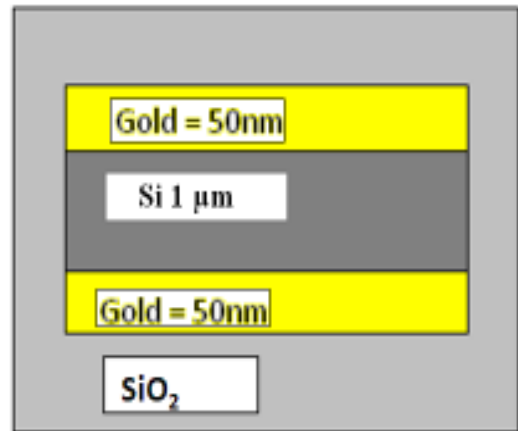


Fig. 2: Cross sectional view of tapered waveguide

The formula for exponential profile is:

$$y = \exp [(\alpha/l)-1]. \text{ Where } l \text{ is the length of the waveguide.}$$

Maximum efficiency obtained for such structure is of the order of 20% and is seen at Si thickness 1 um and for length 1.70um. Best efficiency is obtained for $\alpha = -2.5$.

2. Slot Waveguide:

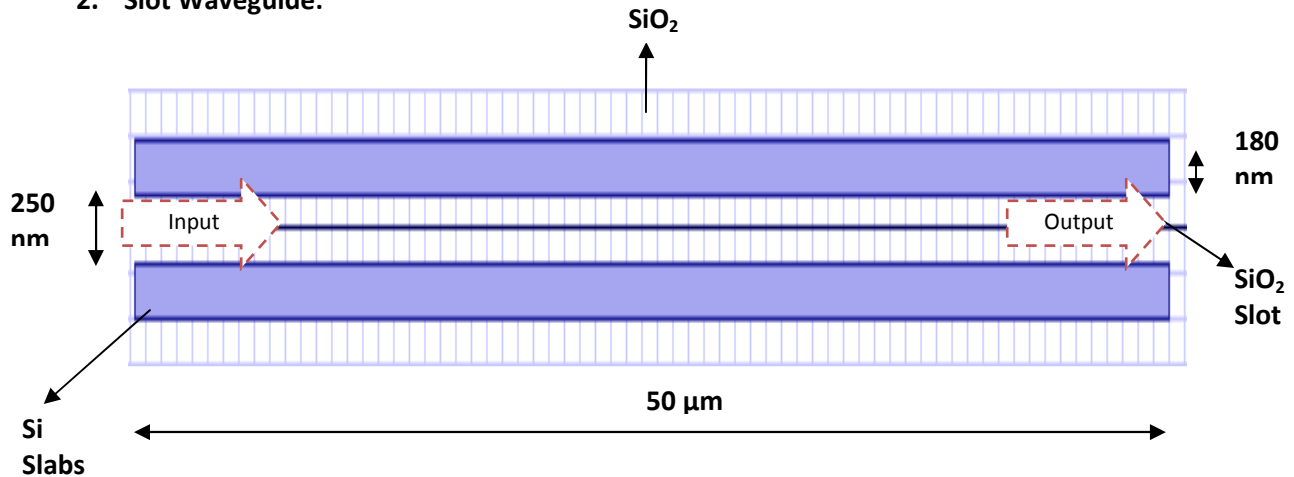
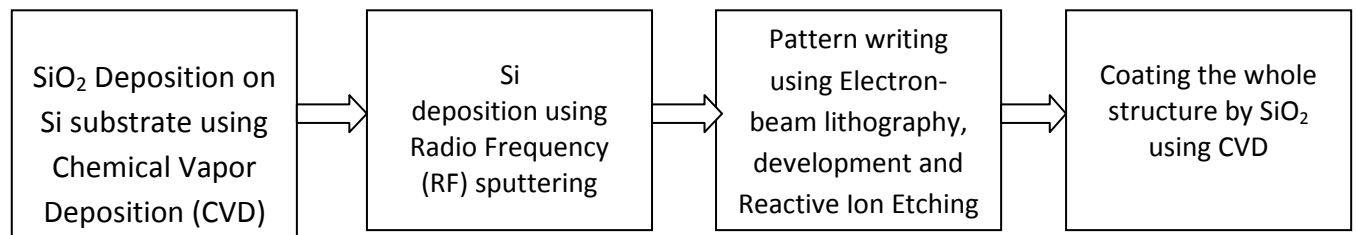


Fig. 3: Slot waveguide

Field confinement obtained near the output was around 15% and was seen at SiO₂ slot width of 250nm formed between a 50µm long and 180nm wide Silicon Slabs. The thickness of these Silicon slabs is 250nm.

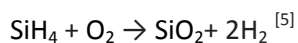
Fabrication:

The fabrication of slot waveguide was done in following steps:



1. SiO₂ Deposition using CVD:

For depositing SiO₂ using CVD, Silane and Oxygen are used, the reaction for the process is



Flow rate for the gasses SiH₄, O₂ and Ar was 150, 13.5, 150 SCCM respectively. Source power was 500W and temperature was 150⁰C

Deposition Rate for SiO₂ for the conditions mentioned above was 28nm/min

2. Si deposition using RF sputtering:

Silicon was deposited using RF magnetron sputtering [6]. In this process Silicon was deposited on SiO₂ Substrate. For this process RF power used was 150W, Ar flow was 30 SCCM and during the process gas pressure was maintained at 1.3x10⁻² mbar. Surface roughness of this Silicon film was 3 nm.

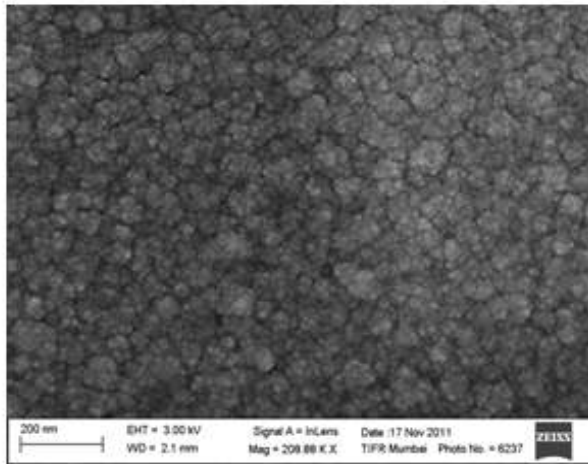


Fig. 4: SEM image of Si deposited using sputtering
Deposition rate of Silicon was 18 nm/min

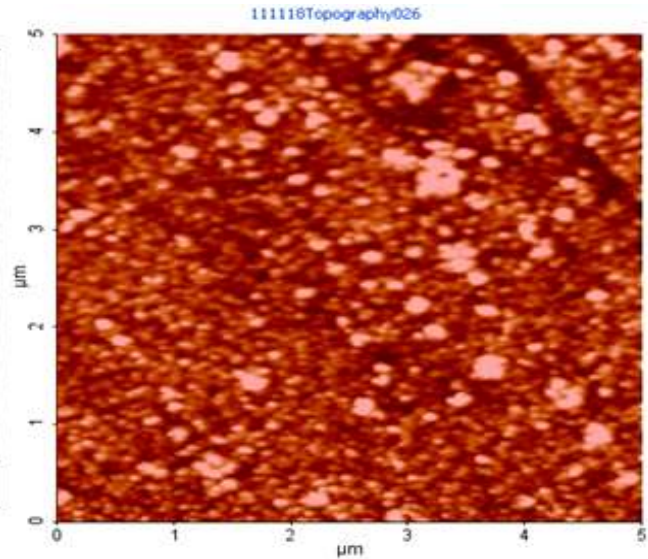


Fig. 5: AFM image of Si deposited using sputtering
(5 μ mX5 μ m)

3. Electron beam lithography:

Steps for E-beam lithography:

1. Sample Preparation:

Sample was heated at 200 $^{\circ}$ C for 30 min to remove any moisture

2. Pre-coating:

IPA was coated on the substrate with speed 1000 rpm and Ramp 500 rpm/s for 10s

3. Resist coating and baking:

Negative resist ma-N 2401 was coated at 3000 rpm and Ramp 300 rpm/s for 30s. The sample was baked at 90 $^{\circ}$ c for 60s.

4. E-beam Exposure and Writing:

For writing the exposure parameters were

Area Dose: 120 μ C/cm 2

Aperture: 30 μ m

EHT: 20 KV

5. Development and RIE:

Ma-D-525 developer was used to develop the sample. The sample was dipped in the developer for 15s and then was rinsed in DI water for 10 min followed by blow drying with N $_2$ followed by RIE.

6. Resist Removal:

O $_2$ plasma was used for the removal of resist.

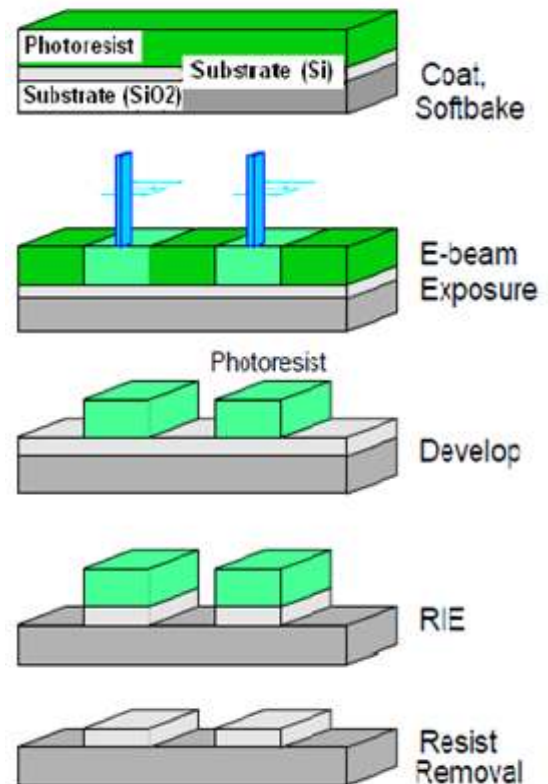


Fig. 5: Process flow for e-beam and RIE

4. Reactive Ion Etching (RIE):

SiF_6 and CHF_3 were used for the etching of Silicon. [7] The flow rate for the gasses was 15 and 40 SCCM, respectively. The ICP source was at 100W and RF power was 75W. Pressure maintained in the chamber during the process was 1.5 Pa. Using this process etch rate of 7nm/s was obtained.

Conclusion:

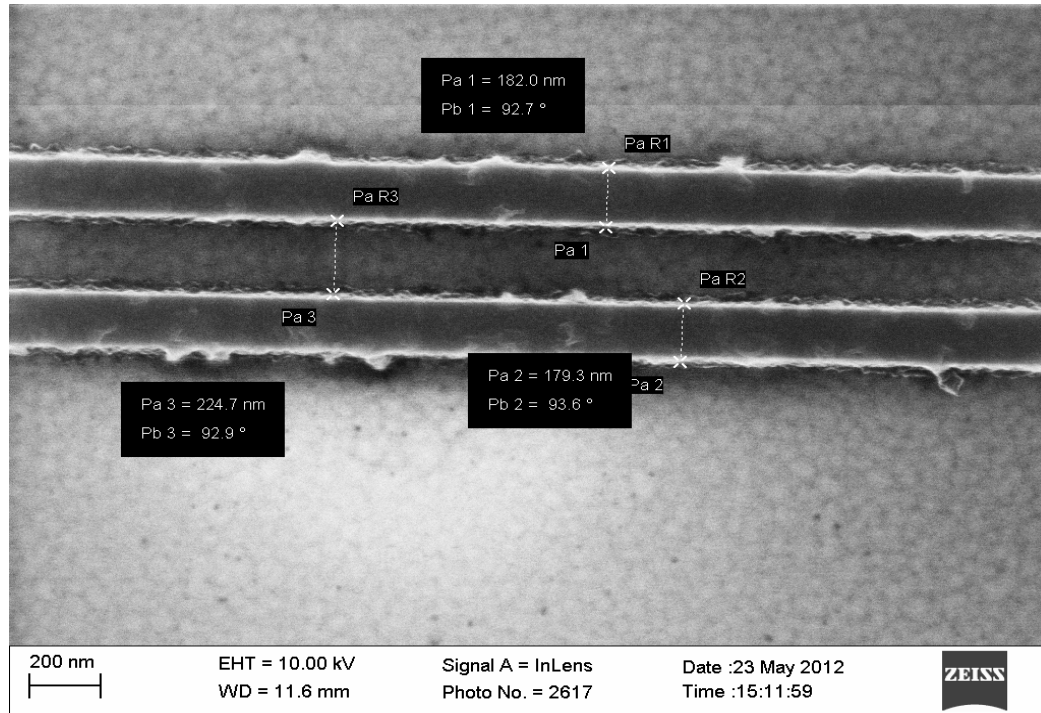


Fig. 6: SEM image of Slot Waveguide

After initial optimization of each of the process steps, we have fabricated slot waveguide. During the fabrication process for the mentioned conditions, the deposition rate of SiO_2 using CVD was found to be 28nm/min. Deposition rate for Silicon using RF magnetron Sputtering was 18nm/min. The processing conditions for the negative resist and Electron Beam Lithography parameters were optimized for Silicon. For the future, testing of these waveguides and fabricating the designed tapered waveguides would be interesting.

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